Marked-up copy of the claims.

21. (Amended) A method of constructing a multi-chip package, comprising:

placing a [fist] first chip package on a first shelf;

electrically attaching said first chip package to [said first shelf] a plurality of shelves;

placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and[,]

electrically attaching said second chip package to said second shelf.

22. (amended) The method of claim 21 further comprising the step of filling said multi-chip package above said second chip package with an encapsulant.

23. (amended) The method of claim 22 wherein said step of placing [a] said second chip package on [a] said second shelf further comprises placing [a] said second chip package on [a] said second shelf with a sealer such that a sealed open cavity below said second shelf protects said first chip package.

24. (amended) The method of claim 21 wherein said step of placing [a] said first chip package further comprises placing a CPU chip package on [a] said first shelf.

25. (amended) The method of claim 21 wherein said step of placing [a] said second chip package further comprises placing a memory cache on [a] said second shelf.

26. (amended) The method of claim 21 wherein said step of electrically attaching said first chip package further comprises wire bonding said first chip package to said [first shelf] plurality of shelves.

27. (amended) The method of claim 21 wherein said step of electrically attaching said second chip package further comprises wire bonding said second chip package to said [second shelf] plurality of shelves.

Marked-up copy of the specification.

Previous title: "STACKED CHIP PACKAGING"
New title: "METHOD OF FABRICATING A STACKED CHIP PACKAGE"

The paragraph on page 13, beginning on line 18 of the specification:

The SRAM cache 74 is mounted to a ceramic substrate 32 through use of solder balls 72 (step 78). A standard flip chip substrate may be used for the SRAM cache 74. An underfill coating (not shown) may be applied (step 80) to further secure the SRAM cache 74 to the substrate 32, a functionality test is performed to verify performance of the SRAM chip (step82). If the SRAM chip is satisfactory, fabrication of the multi-chip package 70 may continue, otherwise the SRAM chip will be replaced.

The paragraph on pages 14 – 15, beginning on page 14, line 18 of the specification:

The multi-chip package 90 can be fabricated in a similar process flow as that discussed above with respect to multi-chip package 70. A CPU die 26 is first attached to a slug 24 (step 98). The slug 24 supporting the CPU die 26 is then attached to the organic package 93, where the CPU die 26 is electrically connected to the package 93 via wire bonds I 28 and 30 (step 100). Note that the organic package 93 is comprised of a series of layers or shelves 14, 16, 18, 20, and 22, and has connector pins 94 staked through (or extending through) the package 93 to allow the multi-chip package 90 to be electrically coupled to other devices (e.g., a PCB). Once the CPU die 26 and slug 24 are attached to the chip package 17, a first encapsulant

fills (step 102) the area 92 above the CPU die 26. The encapsulant (not shown) is generally an epoxy used for environmental protection of the die 26.

The last paragraph on page 17 beginning on line 7 of the specification:

Once any testing is complete, a CPU device 140 is mounted to the base of the package 93 and electrically connected through use of the solder balls 142. Note that ceramic package 17 is comprised of a series of layers or shelves 14, 16, 18, 20, and 22, and has solder balls 122 attached to the surface of the upper shelf 14 to allow the multi-chip package 120 to be electrically coupled to other devices (e.g., a PCB). In this manner, the multi-chip package 118 may be used to mount a plurality of semiconductor devices to, for example, a PCB in a single chip footprint. Standard single package PGA and BGA options have not been capable of supporting multi-chip formats without expanding the footprint of the package. Thus, the present invention provides significant advantages over the prior art.